EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Peter Gallagher on 06/16/2009.

The application has been amended as follows:

Please replace the following claims with the following examiner amendment:

1. A multi-channel integrator comprising:

an integrator input;

an integrator output;

an adder comprising:

a first adder input connected to the integrator input;

a second adder input; and

an adder output;

a delay section comprising:

a delay section input that receives data of a plurality of channels;

a delay section output; and

a plurality of delay elements connected in series between the delay section input and the delay section output, each delay element of the plurality of delay elements delaying the data of each of the plurality of channels and providing an output that is specific to an individual channel of the plurality of channels; and

a feedback line connecting the delay section output to the second adder input;

wherein the adder output is connected to the delay section input; and

further wherein the delay section output is connected to the integrator output.

5. An M channel decimator, wherein M>1, the decimator comprising:

the integrator of claim 1.

15. A multi-channel differentiator comprising:

a differentiator input;

a differentiator output:

a subtractor comprising:

a first subtractor input;

a second subtractor input; and

a subtractor output;

a delay section comprising:

a delay section input connected to the differentiator input, the delay section input receiving data of a plurality of channels;

a delay section output; and

a plurality of delay elements connected in series between the delay section input and the delay section output, each delay element of the plurality of delay elements delaying the data of each of the plurality of channels and providing an output that is specific to an individual channel of the plurality of channels; and

a feedforward line connecting the differentiator input to the first subtractor input;

wherein the delay section output is connected to the second subtractor input; and

wherein the subtractor output is connected to the differentiator output.

26. An N stage, M channel decimator, where M>1, the decimator comprising:

an integrator section comprising:

an integrator section input comprising a multiplexer comprising M multiplexer inputs and a multiplexer output;

an integrator section output; and

N integrators connected in series between the integrator section input and the integrator output, wherein each integrator comprises:

an integrator input;

an integrator output;

an adder comprising:

a first adder input connected to the integrator input;

a second adder input; and

an adder output;

a delay section comprising:

a delay section input;

a delay section output; and M delay elements connected in series between the delay section input and the delay section output, each of the M delay elements delaying data of each of the M multiplexer inputs and providing an output that is specific to an individual channel of the M channels; and

a feedback line connecting the delay section output to the second adder input;

wherein the adder output is connected to the delay section input; and

further wherein the delay section output is connected to the integrator output;

a differentiator section comprising:

a differentiator section input;

a differentiator output; and

N differentiators connected in series between the differentiator input and the differentiator output, wherein each differentiator comprises:

a differentiator input;

a differentiator output:

a subtractor comprising:

a first subtractor input;

a second subtractor input; and

a subtractor output;

a delay section comprising:

a delay section input connected to the differentiator input;

a delay section output; and

M delay elements connected in series between the delay section input and the delay section output; and

a feedforward line connecting the differentiator input to the first subtractor input;

wherein the delay section output is connected to the second subtractor input; and

wherein the subtractor output is connected to the differentiator output; and

a down-sampler comprising a down-sampler input connected to the integrator section output and a down-sampler output connected to the differentiator section input

27. An N stage, M channel interpolator, where M>1, the interpolator comprising:

a differentiator section comprising:

a differentiator section input comprising a multiplexer comprising M multiplexer inputs and a multiplexer output;

a differentiator output; and

N differentiators connected in series between the differentiator input and the differentiator output, wherein each differentiator comprises:

a differentiator input;

a differentiator output:

a subtractor comprising:

a first subtractor input;

a second subtractor input; and

a subtractor output;

a delay section comprising:

a delay section input connected to the differentiator input;

a delay section output; and

M delay elements connected in series between the delay section input and the delay section output, each of the M delay elements delaying data of each of the M multiplexer inputs and providing an output that is specific to an individual channel of the M channels; and

a feedforward line connecting the differentiator input to the first subtractor input;

wherein the delay section output is connected to the second subtractor input; and

wherein the subtractor output is connected to the differentiator output;

an integrator section comprising:

an integrator section input;

an integrator section output; and

N integrators connected in series between the integrator section input and the integrator output, wherein each integrator comprises:

an integrator input;

an integrator output;

an adder comprising:

a first adder input connected to the integrator input;

a second adder input; and

an adder output;

a delay section comprising:

a delay section input;

a delay section output; and

M delay elements connected in series between the delay section input and the delay section output; and

a feedback line connecting the delay section output to the second adder input;

wherein the adder output is connected to the delay section input; and

further wherein the delay section output is connected to the integrator output; and

an up-sampler comprising an up-sampler input connected to the differentiator section output and an up-sampler output connected to the integrator section input.

28. An M channel numerically controlled oscillator, where M>1, the numerically controlled oscillator comprising:

an oscillator input comprising a multiplexer comprising M multiplexer inputs and a multiplexer output;

a sine/cosine generator having a generator input; and

an integrator comprising:

an integrator input connected to the multiplexer output;

an integrator output connected to the generator input;

an adder comprising:

a first adder input connected to the integrator input;

a second adder input; and

an adder output;

a delay section comprising:

a delay section input;

a delay section output; and

M delay elements connected in series between the delay section input and the delay section output, each of the M delay elements delaying data of each of the M multiplexer inputs and providing an output that is specific to an individual channel of the M channels; and

a feedback line connecting the delay section output to the second adder input;

wherein the adder output is connected to the delay section input; and

further wherein the delay section output is connected to the integrator output.

29. A computer program product for performing multi-channel integration on data of a plurality of channels, the computer program product stored on a computer storage media having computer readable code embodied therein, the computer readable code comprising:

computer code that, when executed by a processor, programs a device to create a programmed device, wherein the programmed device comprises:

a multi-channel integrator comprising:

an integrator input;

an integrator output;

an adder comprising:

a first adder input connected to the integrator input;

a second adder input; and

an adder output;

a delay section comprising:

a delay section input;

a delay section output; and

a plurality of delay elements connected in series between the delay section input and the delay section output, each delay element of the plurality of delay elements delaying the data of each of the plurality of channels and providing an output that is specific to an individual channel of the plurality of channels; and

a feedback line connecting the delay section output to the second adder input;

30. A computer program product for performing multi-channel differentiation on data of a plurality of channels, the computer program product stored on a computer storage media having

computer readable code embodied therein, the computer readable code comprising:

computer code that, when executed by a processor, programs a device to create a programmed device, wherein the programmed device comprises:

a multi-channel differentiator comprising multi-channel differentiator comprising:

a differentiator input;

a differentiator output:

a subtractor comprising:

a first subtractor input;

a second subtractor input; and

a subtractor output;

a delay section comprising:

a delay section input connected to the differentiator input;

a delay section output; and

a plurality of delay elements connected in series between the delay section input and the delay section output, each delay element of the plurality of delay elements delaying the data of each of the plurality of channels and providing an output that is specific to an individual channel of the plurality of channels; and

a feedforward line connecting the differentiator input to the first subtractor input;

wherein the delay section output is connected to the second subtractor input; and

wherein the subtractor output is connected to the differentiator output.

The following is an examiner's statement of reasons for allowance:

The prior art of record does not teach or suggest each delay element of the plurality of delay elements delaying each of the M channel's data and providing an output that is specific to an individual channel of the M channels; as recited in independent claims 1, 15, and 26-30.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL YAARY whose telephone number is (571)270-1249. The examiner can normally be reached on Mon-Fri 9 a.m.-5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on 571-272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. Y./
Examiner, Art Unit

/Lewis A. Bullock, Jr./

Supervisory Patent Examiner, Art Unit 2193